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L1: Entry 3 of 3 File: USPT Nov 28, 2000

DOCUMENT-IDENTIFIER: US 6153448 A
TITLE: Semiconductor device manufacturing method

US Patent No. (1):
6153448

Brief Summary Text (6):
In FIGS. 9 and 10, reference numeral 80 designates a semiconductor pellet which comprises a semiconductor substrate 1 formed with semiconductor devices 91, wirings 92, electrode pads 93, a passivation film 94, etc., as shown in FIG. 11, for example. Reference numeral 2 designates a tape insulation layer bonded on to the passivation film on the pellet 80 so as to cover regions thereof except a peripheral region, and reference numeral 3 designates a plurality of wiring patterns formed on the tape insulation layer 2, some of the patterns being electrically connected to a part of a plurality of electrode pads formed on the semiconductor pellet although not shown.

Brief Summary Text (7):
Reference numeral 6 designates external electrodes in the form of balls provided on a part of the wiring patterns 3 in electrical connection thereto. Reference numeral 8 designates bonding wires for connection between electrode pads 7 formed on the peripheral area of the pellet 80, i.e., the region of the pellet 80 which is not covered by the tape insulation layer 2 and the wiring patterns 3 on the tape insulation layer adjacent thereto. Reference numeral 9 designates resin bonded and hardened so as to seal the bonding wires 8 and the electrode pads 7 and wiring patterns 3 to which bonding wires are connected by bonding on both ends thereof.

Brief Summary Text (22):
Further, according to the present invention, a method for manufacturing a semiconductor device comprising the steps of: forming a plurality of chip regions including a plurality of electrode pads on a semiconductor wafer; forming a barrier metal layer on the semiconductor wafer and performing etching to selectively leave the barrier metal on the electrode pad in each of the chip region and in a predetermined region surrounding the same; forming line grooves to a depth which is halfway the thickness of the substrate between the chip regions of the semiconductor wafer; forming an insulation layer serving also as a sealing layer having openings for via holes in correspondence to the arrangement of the barrier metal; forming wiring patterns including via hole wiring portions connected to the barrier metal at the bottom of the openings for via holes and including land portions connected thereto and arranged regularly in the form of a matrix in positions on the tape insulation layer offset from the via hole portions; mounting external electrodes in the form of balls on the land portions of the wiring patterns; and cutting the wafer with a dicing saw along the center lines of the line grooves to divide it into semiconductor devices in a chip-size package structure including a ball grid array electrode.

Brief Summary Text (23):
In the method for manufacturing a semiconductor device, at the step of forming the insulation layer serving also as a sealing layer, a thermally hardened epoxy tape formed with the openings for via holes using a punching process may be applied to the semiconductor wafer using a thermo-compression bonding process.

Brief Summary Text (24):
In the method for manufacturing a semiconductor device, a metal core material may be added to the thermally hardened epoxy tape.

Detailed Description Text (5):
Reference numeral 12 designates an insulation layer serving also as a sealing layer formed on the peripheral surface portions of the barrier metal layers 11 and the exposed surface portions of the passivataion film. In this embodiment, the insulation film 12 is constituted by a thermally hardened epoxy tape which is formed with via hole portions in association with the arrangement of the plurality of barrier metal layers 11 using a punching process and which is applied using a thermo-compression bonding process.

Detailed Description Text (22):
Next, as shown in FIG. 4A, an insulation layer 12 serving also as a sealing layer is formed by applying, using a thermo-compression bonding process, a thermally hardened epoxy tape having openings 17 for via holes formed by punching in association with the arrangement of the plurality of barrier metal layers 11. As a result, the insulation layer 12 covers the entire surface of the individual chip regions and major parts of the sides of the individual chip regions except the barrier metal layers exposed at the openings 17. When high reliability is required, a metal core material may be advantageously added to the thermally hardened epoxy tape.

Detailed Description Text (27):
Thereafter, as indicated by the broken line in FIG. 4C, a dicing saw is used along the center lines of the half-cut line grooves to perform cutting. Thus, the semiconductor device is divided into semiconductor devices having a chip-size package structure including a BGA (ball grid array) electrode.

Detailed Description Text (30):
The manufacturing steps according to the second embodiment are different from the manufacturing steps according to the first embodiment in that the step of applying a tape for forming the insulation layer 12 serving also as a sealing layer is replaced with the formation of an insulation film by applying a liquid material such as photosensitive epoxy which is followed by patterning using a photographic process to form openings for via holes in the insulation layer. Other processing steps are the same as those in the first embodiment and will not be described.

Detailed Description Text (39):
Thereafter, cutting is performed by using a dicing saw along the center lines of the half-cut line grooves to divide the semiconductor device into semiconductor devices having a chip-size package structure having a schematic sectional configuration as shown in FIG. 6F.

Other Reference Publication (1):
Anderson et al., Extended Pad for Testing Package Parts, IBM Technical Disclosure Bulletin, vol. 27 No. 7B, pp. 4210-4211, Dec. 1984.

CLAIMS:

1. A method for manufacturing a semiconductor device comprising the steps of:

forming a plurality of chip regions including a plurality of electrode pads on a semiconductor wafer;

forming a barrier metal layer on said semiconductor wafer and performing etching to selectively leave the barrier metal on the electrode pad in each of said chip region and in a predetermined region surrounding the same;

forming line grooves to a depth which is halfway the thickness of the substrate between the chip regions of said semiconductor wafer;

forming an insulation layer serving also as a sealing layer having openings for via holes in correspondence to the arrangement of said barrier metal;

forming wiring patterns including via hole wiring portions connected to said barrier metal at the bottom of said openings for via holes and including land portions connected thereto and arranged regularly in the form of a matrix in positions on the tape insulation layer offset from said via hole portions;

mounting external electrodes in the form of balls on the land portions of said wiring patterns; and

cutting the wafer with a dicing saw along the center lines of said line grooves to divide it into semiconductor devices in a chip-size package structure including a ball grid array electrode.

2. A method for manufacturing a semiconductor device according to claim 1, wherein at said step of forming the insulation layer serving also as a sealing layer, a thermally hardened epoxy tape formed with said openings for via holes using a punching process is applied to said semiconductor wafer using a thermo-compression bonding process.

3. A method for manufacturing a semiconductor device according to claim 2, wherein a metal core material is added to said thermally hardened epoxy tape.